Remarks

Claims 1-32 are pending in the application and are presented for reconsideration. Claims 1, 12, and 29 have been amended; Claim 10 has been cancelled; and Claims 2-9, 11, 13-28, and 30-32 remain in the application unchanged. No new matter has been added.

Claim Rejections

Claims 1-3, 5, 8, 9, 12-20, 29 and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Stevens (U.S. Pat. No. 5,465,065).

Claims 6, 7, 21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Stevens in view of Horowitz et al. ("The Art of Electronics", Cambridge University Prescriptions, 1980, pages 343-344).

Claims 4, 11, 24-28 and 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Stevens in view of Miura (U.S. Pat. No. 6,756,833).

Claims 23 and 31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Stevens in view of Baumann (U.S. Pat. No. 5,744,992).

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Response to Rejections of Claims

The Applicant wants to bring to the attention of the Examiner that in reviewing Claim 10 with attention to Fig. 4, the features as recited in Claim 10 incorrectly recited "each AND gate having ... a second input configured to be driven by *the output of the logic memory element of the first rank* associated with the delay unit immediately preceding the delay unit associated with the AND gate". Claims 1, 12, and 29 instead recite "each AND gate having ... a second input configured to be driven by the output of the *AND gate* associated with the delay unit immediately preceding the delay unit associated with the AND gate", which is consistent with the circuit shown in FIG. 4 and the Specification, page 7, lines 17-20.

Independent Claims 1, 12, and 29 have been amended to include all of the limitations of Claim 10 with the above stated correction. Accordingly, since none of the prior art, taken alone or in any combination, teach or suggest the limitation "a plurality of AND gates, each AND gate being associated with one of the series of delay units, each AND gate having an output configured to drive the data input of the logic memory element of the first rank associated with the delay unit associated with the AND gate, each AND gate having a first input configured to be driven by the output of its associated delay unit and a second input configured to be driven by the output of the AND gate associated with the delay unit immediately preceding the delay unit associated with the AND gate, the second input of the AND gate associated with a first delay unit of the series of delay units being configured to be driven by a logic HIGH", **Claim 1** is now believed in position for allowance. The Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. § 103(a) rejection of Claim 1.

Claims 2-9 and 11 each depend from independent base claim 1 and add further limitations. For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claims 2-9 and 11 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 2-9 and 11 should be withdrawn.

Claims 12 and 29 have been amended to recite limitations similar to that of Claim 1, in particular, "a plurality of means for forming a logical AND function, each logical AND function means being associated with one of the plurality of delayed inverted clock signals, each logical AND function means generating a logical AND signal representing a logical AND of its associated delayed inverted clock signal and the logical AND signal generated by the logical AND function means associated with the immediately preceding delayed inverted clock signal if an immediately preceding delayed inverted clock signal exists" and "forming a plurality of logical AND functions, each logical AND function being associated with one of the plurality of delayed inverted clock signals, each logical AND function generating a logical AND signal representing a logical AND of its associated delayed inverted clock signal and the logical AND signal generated by

the logical AND function associated with the immediately preceding delayed inverted clock signal if an immediately preceding delayed inverted clock signal exists", respectively. For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claims 12 and 29 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejections of Claims 12 and 29 should also be withdrawn.

Claims 13-28 and 30-32 respectively depend from independent base claims 12 and 29 and add further limitations. For at least the same reasons that Claims 12 and 29 are not shown, taught, or disclosed by the cited references, Claims 13-28 and 30-32 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 13-28 and 30-32 should be withdrawn.

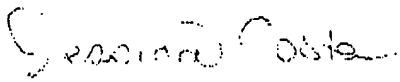
Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 1-9 and 11-32 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

November 21, 2005



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